IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): G.A. Bouchard et al.
Case: 3-7-4-4-7-2
Serial No.: 10/029,679
Filing Date: December 21, 2001
Group: 2152
Examiner: Lan Dai T. Truong

Title: Methods and Apparatus for Using Multiple Reassembly Memories for Performing Multiple Functions

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REPLY BRIEF

Commissioner for Patents
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Sir:

Appellants present the following remarks addressing the arguments raised in the Examiner's Answer dated May 22, 2007. Appellants incorporate herein all remarks previously presented, including those presented in Appellants' Appeal Brief dated January 16, 2007.

ARGUMENTS

The Examiner's Answer reiterates many of the arguments previously raised by the Examiner and which are fully addressed in Appellant's Appeal Brief. Thus, the present Reply Brief reiterates Appellants arguments to the various grounds of rejection first made in Appellants' Appeal Brief, followed by Appellants' responses to the Examiner's latest comments (made in the "Response to Arguments" section of the Examiner's Answer at pages 10-16).

(I) Whether claims 1-3, 6 and 11-20 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 5,623,494 (hereinafter "Rostoker") in view of U.S. Patent No. 6,934,760 (hereinafter "Westbrook").

Regarding the §103(a) rejections, Appellants assert that the various references, alone or in combination, fail to teach or suggest all of the limitations of claim 1-9 and 11-20, as will be explained below. Furthermore, with regard to the combinations of the various references, Appellants assert that such combinations are improper, as will be explained below.

The Examiner cites Rostoker in combination with Westbrook in rejecting independent claims 1, 15 and 18. More particularly, the Examiner cites portions of Rostoker as disclosing certain limitations of the independent claims, and cites portions of Westbrook as disclosing certain other limitations of the independent claims. Below, Appellants explain how such portions of Rostoker and Westbrook fail to teach or suggest what the Examiner contends that they teach or suggest. While Appellants may refer from time to time to each reference alone in describing its deficiencies, it is to be understood that such arguments are intended to point out the overall deficiency of the cited combination.

In characterizing the Rostoker reference as allegedly meeting certain limitations of claim 1, the Examiner relies primarily on the abstract, lines 1-28; column 3, lines 34-47; column 4, lines 20-26; column 6, lines 48-67; and figure 2. However, the relied-upon portions of Rostoker fail to teach or suggest the limitations as alleged. The relied-upon portions of Rostoker state that each ATM termination unit 50 includes a processor for segmenting and reassembling the ATM cells and that each ATM terminal unit interfaces with a host unit 102. The Examiner seems to consider two of the

host units to be the claimed "first processing circuitry" and "second processing circuitry," as well as the "first memory circuitry" and "second memory circuitry." Further, the Examiner seems to consider two of the ATM terminal units to be the claimed "first reassembly circuitry" and "second reassembly circuitry."

However, even assuming this is the case for the sake of argument, no where does Rostoker disclose that the second reassembly circuitry, associated with the second processing circuitry, reassembles at least a portion of the same segments of packets reassembled by the first reassembly circuitry into reassembled packets, the segments to be reassembled being related to a second function (whereas the segments reassembled by the first reassembly circuitry are related to a first function), as recited in the independent claims. That is, no where does Rostoker state that one ATM terminal unit reassembles at least a portion of the same segments of packets reassembled by another ATM terminal unit.

The Examiner states on page 3 of the final Office Action that "applicant does not clearly disclose if the first function and second function are distinct; so they could execute the same job/or task." However, this is not relevant to the claimed limitation. The claimed limitations recites that the second reassembly circuitry reassembles at least a portion of the same segments of packets reassembled by the first reassembly circuitry. The claim expressly recites a limitation with respect to the sameness of the packets, not the sameness of the first and second functions.

The Westbrook reference fails to supplement the above-noted deficiencies of Rostoker as applied to claim 1.

In characterizing the Westbrook reference as allegedly meeting certain limitations of claim 1, the Examiner relies primarily on column 7, lines 22-27 and lines 55-60, of Westbrook. However, the relied-upon portions of Westbrook fail to teach or suggest the limitations as alleged. The relied-upon portions of Westbrook appear to relate to distributed resequencing and/or reassembling components resequencing and/or reassembling packets. For example, Westbrook at column 7, lines 22-27, provides as follows:

> Moreover, these distributed resequencing and/or reassembly components 203A-N may resequence and/or reassemble a single stream of packets, or typically in a large system simultaneously resequence and/or reassemble one or more streams of packets.

In addition, Westbrook, at column 7, lines 55-60, provides as follows:

> Distributed resequencing and/or reassembly components 203A-N coordinate the resequencing and/or reassembly process(es) typically by sharing information as to what packets are currently held by each of the distributed resequencing and/or reassembly components 203A-N, and coordinating the sending of packets over a packet merge bus 209 (or other communications mechanism) to produce one or more streams of resequenced and/or reassembled packets.

There is no description in the relied-upon portion of Westbrook relating to, for example, the claimed features of: "at least a portion of the reassembled packets stored in the first memory circuitry and the second memory circuitry are the same."

That is, while Westbrook describes multiple components for resequencing and/or reassembling packets, it is clear that Westbrook is not stating that any two components reassemble the same packets. In fact, it is clear from Figure 2A and 2b of Westbrook (and the related textual description) that Westbrook is solving the "out-of-sequence" problem (see column 1 of Westbrook) that occurs when individual packets from one or more data streams are separated so they can be individually routed on different network paths in order to get to a single destination more efficiently. Thus, distributors 200 shown in Figures 2A and 2B are understood to distribute different packets to each component 203. In fact, if the same packets could be distributed to each component (as the Examiner seems to suggest), there would be no need for the components to communicate between one another as to which packets each component received (see column 8, lines 9-11 of Westbrook).

In the Advisory Action, the Examiner again states that Westbrook "discloses method for sending packets of data into multiple 'reassembly units' those [sic] are equivalent to 'reassembly circuitries', then the 'reassembled packets' those [sic] are equivalent to 'portion of segments of packets' sent to another reassembly unit, see (column 4, lines 50-60, lines 1-25; column 5, lines 1-13; column 7, lines 22-27, 55-60; column 3, lines 40-55)." Furthermore, the Examiner again states in the Advisory Action that "Applicant does not state that the first memory circuitry and the second memory circuitry are distinct as claimed," and points to column 5, lines 1-12 of Westbrook as disclosing at least a portion of the reassembled packets stored in the first memory circuitry and the

second memory circuitry are the same. Again, as noted above, while Westbrook describes multiple components for resequencing and/or reassembling packets, Westbrook does not state that any two components reassemble the same packets.

In the Examiner's Answer, the Examiner refers to Westbrook at column 4, lines 1-47, column 6, lines 55-60, abstract, and FIGS. 1B and 1C as teaching or suggesting "at least second reassembly circuitry, associated with the second processing circuitry, for reassembling at least a portion of the same segments of packets reassembled by the first reassembly circuitry into reassembled packets, the segments to be reassembled being related to the second function." Although Westbrook refers to reassembly components, Westbrook refers to transmitting smaller packets over a common bus or link in a coordinated fashion as to produce the original larger packet, which does not disclose reassembling at least a portion of the same segments of packets reassembled by the first reassembly circuitry into reassembled packets. Also, no where in the relied-upon portions of Westbrook does Westbrook teach or suggest of the segments to be reassembled being related to the second function.

The Rostoker reference fails to supplement the above-noted deficiencies of Westbrook as applied to claim 1. Accordingly, it is believed that the combined teachings of Rostoker and Westbrook fail to meet the limitations of claim 1.

Also, the Examiner has failed to identify a cogent motivation for combining Rostoker and Westbrook in the manner proposed. The Examiner provides the following statement of motivation at page 4, second paragraph of the Office Action:

> Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Westbrook's ideas of a plurality of reassembly components may reassemble a single stream of packets with Rostoker's system in order to provide an improved reassembling system: (Rostoker: column 3, lines 14-26)

In addition, the Examiner provides the following statement of motivation at page 11, last paragraph of the Examiner's Answer:

> In this case, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Westbrook's ideas of reassembly the reassembled packets through a plurality of reassembly components into Rostoker's

> system in order to save resources and development time, to minimize bandwidth utilization, and to provide a higher rate packets transmitting system, see (Westbrook: column 1, lines 37-60).

Appellants respectfully submit that the Examiner's explanation is a conclusory statement of the sort rejected by both the Federal Circuit and the U.S. Supreme Court. See KSR v. Teleflex, 127 S.Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (U.S., Apr. 30, 2007), quoting In re Kahn, 441 F. 3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."). There has been no showing in the present §103(a) rejection of claim 1 of objective evidence of record that would motivate one skilled in the art to combine Rostoker and Westbrook to produce the particular limitations in question. Rather, the above-quoted statement of motivation provided by the Examiner appears to be a conclusory statement of the type ruled insufficient in the KSR case.

For at least these reasons, Appellants assert that independent claim 1 is patentable over the Rostoker/Westbrook combination. Independent claims 15 and 18 include limitations similar to those of claim 1, and are therefore believed patentable for reasons similar to those described above with reference to claim 1. Furthermore, Appellants assert that the claims which depend from claim 1 are patentable over the Rostoker/Westbrook combination not only for the reasons given above with respect to claim 1, but also because such dependent claims recite patentable subject matter in their own right, as will be set out below.

Regarding claims 2, 16 and 19, the Rostoker/Westbrook combination does not teach or suggest "the first processing circuitry, the first reassembly circuitry, the first memory circuitry, the second processing circuitry, the second reassembly circuitry and the second memory circuitry are implemented on an integrated circuit." The Examiner again states that "applicant does not clearly disclose if first function and second function are distinct; so they could execute the same job/or task," at page 5, first paragraph of the final Office Action. As noted above, this is not relevant to the claimed limitation. Independent claims 1, 15 and 18, from which claims 2, 16 and 19 depend from respectively, recite that the second reassembly circuitry reassembles at least a portion of the

same segments of packets reassembled by the first reassembly circuitry, which is a limitation with respect to the sameness of the packets, not the sameness of the first and second functions.

Regarding claims 3, 17 and 20, Rostoker does not teach or suggest "the first processing circuitry, the first reassembly circuitry and the first memory circuitry are implemented on a first integrated circuit, and the second processing circuitry, the second reassembly circuitry and the second memory circuitry are implemented on a second integrated circuit." As noted above, assuming for the sake of argument that the host units of Rostoker are the claimed first and second processing circuitry as well as the first and second memory circuitry, and the ATM terminal units are the claimed first and second reassembly circuitry, no where does Rostoker state that one ATM terminal unit reassembles at least a portion of the same segments of packets reassembled by another ATM terminal unit.

Regarding claim 11, neither Rostoker nor Westbrook teach or suggest of "parsing circuitry... for parsing information from the received packets for use by the first reassembly circuitry and the second reassembly circuitry in respectively reassembling the packets."

In the Examiner's Answer, the Examiner states that parsing circuitry is inherently included in Westbrook's system in order to parse orders of packets for reassembling packets back into the original larger packets (column 3, lines 37-59; column 4, lines 1-29). (Examiner's Answer, page 13, second paragraph). However, Westbrook does not contain the disclosure which is necessary to support a rejection of a claim on the basis of inherency. According to the Court of Customs and Patent Appeals (CCPA), "'[i]nherency does not mean that a thing might be done, or that it might happen, ...; but it must be disclosed, if inherency is claimed, that the thing will necessarily happen.'" *In re Draeger et al.*, 150 F.2d 572, 574 (CCPA 1945) (emphasis supplied). Furthermore, well settled law "requires that inherency may not be established by possibilities and probabilities . . . [t]he evidence must show that the inherency is necessary and inevitable." *Interchemical Corp. v. Watson*, 145 F.Supp. 179, 182, 111 USPQ 78, 79 (D. D.C. 1956) (emphasis supplied), *aff'd*, 251 F.2d 390, 116 USPQ 119 (D.C. Cir. 1958).

Appellants assert that there is no reasonable basis for an assertion that Westbrook's system necessarily includes parsing circuitry. "In relying upon the theory of inherency, the examiner must

provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). No such basis and/or technical reasoning has been provided by the Examiner.

(II) Whether claim 4 is unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 4,149,243 (hereinafter "Wallis").

Appellants assert that claim 4, which depends from claim 1, is patentable over the Rostoker/Westbrook/Wallis combination not only for the reasons given above with respect to claim 1, but also because claim 4 recites patentable subject matter in its own right.

It is also asserted that the motivation set forth by the Examiner to combine Wallis with Rostoker and Westbrook is insufficient under KSR (cited above).

(III) Whether claim 5 is unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 4,593,357 (hereinafter "Ostrand").

Appellants assert that claim 5, which depends from claim 1, is patentable over the Rostoker/Westbrook/Ostrand combination not only for the reasons given above with respect to claim 1, but also because claim 5 recites patentable subject matter in its own right.

It is also asserted that the motivation set forth by the Examiner to combine Ostrand with Rostoker and Westbrook is insufficient under KSR (cited above).

(IV) Whether claim 7 is unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 6,058,114 (hereinafter "Sethuram").

Appellants assert that claim 7, which depends from claim 1, is patentable over the Rostoker/Westbrook/Sethuram combination not only for the reasons given above with respect to claim 1, but also because claim 7 recites patentable subject matter in its own right.

It is also asserted that the motivation set forth by the Examiner to combine Sethuram with Rostoker and Westbrook is insufficient under KSR (cited above).

(V) Whether claims 8 and 9 are unpatentable under 35 U.S.C. §103(a) over Rostoker and Westbrook in view of U.S. Patent No. 6,483,839 (hereinafter "Gemar").

Appellants assert that claims 8 and 9, which depend from claim 1, are patentable over the Mishra/Tenev combination not only for the reasons given above with respect to claim 1, but also because such dependent claims recite patentable subject matter in their own right.

It is also asserted that the motivation set forth by the Examiner to combine Gemar with Rostoker and Westbrook is insufficient under KSR (cited above).

In view of the above, Appellants believe that claims 1-9 and 11-20 are in condition for allowance, and respectfully request withdrawal of the §103(a) rejections.

Respectfully submitted,

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